2/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03854268 INSPEC Abstract Number: B91023993, C91025140
Title: The development of a SPICE model to predict the cross-talk reduction of coupled lines
Author(s): Ladd, D.N.; Costache, G.I.
Author Affiliation: Dept. of Electr. Eng., Ottawa Univ., Ont., Canada
Conference Title: Symposium on Antenna Technology and Applied Electromagnetics 1990 Conference Proceedings. First Edition p.761-5
Publisher: ANTEM, Winnipeg, Man., Canada
Publication Date: 1990 Country of Publication: Canada 787 pp.
ISBN: 0 9692563 2 9
Conference Date: 15-17 Aug. 1990 Conference Location: Winnipeg, Man., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: In high speed and wideband electronic circuit applications, it is desirable to minimize the cross-talk between **parallel** tracks on the printed **circuit board** . This paper presents a technique using **vias**, with which the cross-talk can be reduced by 50 to 90%. A SPICE model combined with the finite element method is developed to predict the performance and is validated with experimental results. (3 Refs)
Subfile: B C
Descriptors: circuit layout CAD; **crosstalk**; finite element analysis ; interference suppression; printed circuit design; strip lines
Identifiers: **crosstalk** reduction; coupled lines; **parallel** tracks; printed **circuit board**; **vias**; SPICE model; finite element method
Class Codes: B2210B (Printed circuit layout and design); B1130B (Computer-aided circuit analysis and design); B1310 (Waveguides); C7410D (Electronic engineering)

2/9/15 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

03714254 **Image available**
SEMICONDUCTOR PACKAGE

PUB. NO.: 04-079354 [JP 4079354 A]
PUBLISHED: March 12, 1992 (19920312)
INVENTOR(s): MINAMI KOJI
ARAI HITOSHI
MAEDA AKITSUGU
KANO TAKESHI
HIGUCHI TORU
APPLICANT(s): MATSUSHITA ELECTRIC WORKS LTD [000583] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-195195 [JP 90195195]
FILED: July 23, 1990 (19900723)
INTL CLASS: [5] H01L-023/12; H01L-025/00
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JOURNAL: Section: E, Section No. 1226, Vol. 16, No. 297, Pg. 54, June 30, 1992 (19920630)

ABSTRACT

PURPOSE: To eliminate electric noise irrespective of high density, miniaturization of a conductor circuit by providing a semiconductor element placing part on the exposed surface of a laminated plate of printed circuit boards formed of metal foil-plated laminated boards, and providing a high permittivity element in the plate.

CONSTITUTION: High permittivity elements 5 are arranged in **through holes** 4 of a laminated plate 2 formed substantially **parallel** to a plurality of **through- holes** 3 of a printed **circuit board** 1 between the holes 3. A semiconductor element placing part 8 is formed in a recess state substantially at the center of the board 1. Since the elements 5 are not arranged on the same surface as a conductor circuit 7 arranged on the surface of the board 1, they do not disturb high density, miniaturization of the circuit 7. Accordingly, the elements each having large electrostatic capacity are arranged in the plate between the conductor circuits irrespective of the high density, miniaturization of the conductor circuit to absorb **crosstalk** charge between the circuits, noise charge to the elements, thereby eliminating **crosstalk**, noise.
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PLEASE ENTER A COMMAND OR BE LOGGED OFF IN 5 MINUTES

2/9/14 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03925197 **Image available**
MULTILAYER **CIRCUIT BOARD**

PUB. NO.: 04-290297 [JP 4290297 A]
PUBLISHED: October 14, 1992 (19921014)
INVENTOR(s): SAKATA TOSHIYASU
YASUDA MITSURU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-052962 [JP 9152962]
FILED: March 19, 1991 (19910319)
INTL CLASS: [5] H05K-003/46
JAPIO CLASS: 42.1 (ELECTRONICS -- Electronic Components)
JOURNAL: Section: E, Section No. 1327, Vol. 17, No. 101, Pg. 79, March 02, 1993 (19930302)

ABSTRACT

PURPOSE: To reduce a **crosstalk** noise in a **via** of a multilayer **circuit board** formed by laminating a plurality of boards, and connecting inner layer patterns of the boards through **vias** passing through the boards.

CONSTITUTION: Pads arranged on an upper surface of a board of an uppermost layer formed by laminating a plurality of boards, first **vias** connected at each one end to a pad and so arranged at the other at a predetermined pitch as to pass the board, second **vias** arranged in **parallel** with the first **vias**, and a **via** connecting pattern so provided on a predetermined layer as to connect the second **vias** to the predetermined **vias** of the first **vias**, are provided. An interval larger than the pitch is formed between the first **vias** nearest the arranging positions of the second **vias** and the arranging positions of the second **vias**. 1-1,1-2,1-3,1-N: board, 2: upper surface, 3: pad, 4: first **via**, 4-1: predetermined **via**, 5: second **via**, 6: **via** connecting pattern.